Application No.: 10/047,809
Amendment dated: June 8, 2005
Reply to Office Action dated: March 8, 2005

REMARKS/ARGUMENTS

Claims 1-20 are pending in the application.

Claims 1-7 and 15-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 9-14 stand rejected under 35 U.S.C. §101 because they are directed to non-statutory subject matter. Claims 1, 9, and 15 stand rejected under 35 U.S.C. §102(b) as being anticipated by "Simultaneous Multithreading: A Platform for Next-Generation Processor" by Eggers et al. (Hereinafter "Eggers"). Claim 2 stands rejected under 35 U.S.C. §103(a) as unpatentable over Eggers. Claims 3-8, 10-14, and 16-20 stand rejected under 35 U.S.C. §103(a) as unpatentable over Eggers in view of what the Examiner refers to as applicants' admitted prior art (Hereinafter "AAPA").

Claim Rejections Under 35 U.S.C. §112

Claims 1-7 and 15-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-7 and 15-20 have been amended per the Examiner's request.

Claim Rejections Under 35 U.S.C. §101

Claims 9-14 stand rejected under 35 U.S.C. §101 because they are directed to non-statutory subject matter. Claims 9-14 have been amended per the Examiner's suggestions.

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Claim Rejections Under 35 U.S.C. §102(b)

Claims 1, 9, and 15 stand rejected under 35 U.S.C. §102(b) as being anticipated by Eggers. Eggers discloses simultaneous multithreaded processors that use either multithreaded parallel programs or individual, independent programs in a multiprogramming workload.

Eggers fails to teach or suggest determining whether a multi-threading processor is wide enough to execute a first thread and a second thread in parallel, as recited in claims 1, 9, and 15. Eggers states:

> Figure 1c shows how each cycle an SMT processor selects instructions for execution from all threads. It exploits instruction-level parallelism by selecting instructions from any thread that can (potentially) issue. The processor then dynamically schedules machine resources among the instructions, providing the greatest chance for the highest hardware utilization. If one thread has high instruction-level parallelism, that parallelism can be satisfied; if multiple threads each have low instruction-level parallelism, they can be executed together to compensate. In this way, SMT can recover issue slots lost to both horizontal and vertical waste.

(Eggers, p. 13, left column, last full paragraph).

In other words, Eggers combines the processing of threads only for those threads that have a low level of parallelism (i.e., threads where the instructions of the thread cannot be processed simultaneously). The width of the processor is not taken into account. As at least this element is not disclosed, Eggers fails to anticipate claims 1, 9, and 15.

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Claim Rejections Under 35 U.S.C. §103(a)

Claim 2 stands rejected under 35 U.S.C. §103(a) as unpatentable over Eggers. As stated above, Eggers fails to teach or suggest determining whether a multi-threading processor is wide enough to execute a first thread and a second thread in parallel, as claimed in claim 1. As at least this element is not taught by Eggers, claim 1, and by its dependency claim 2, are not obvious under Eggers.

Claims 3-8, 10-14, and 16-20 stand rejected under 35 U.S.C. §103(a) as unpatentable over Eggers in view of the AAPA. As stated above, Eggers fails to teach or suggest determining whether a multi-threading processor is wide enough to execute a first thread and a second thread in parallel, as claimed in claims 1, 9, and 15. The AAPA does not correct this deficiency. Further, use of the AAPA implicitly involves using impermissible hindsight as the Office Action is using the Applicant's own observations in combining elements of the AAPA with Eggers.

Additionally, Eggers specifically teaches away from using an in-order processor, as required by claims 3, 11, and 17, and by their dependency claims 4-8, 12-14, and 18-20. As mentioned above, Eggers determines whether to execute threads based on the threads' parallelism, or whether multiple instructions in a thread may be executed simultaneously (i.e. out of order). While some threads may be processed in order, that is based on the threads and not on the processor.

As at least these elements are not taught by Eggers and the AAPA, and Eggers and the AAPA are impermissibly combined, claims 1, 9, and 15, and by their dependency claims 3-8, 10-14, and 16-20, are not obvious under Eggers.

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Request for Allowance

It is believed that this Amendment places the application in condition for allowance, and early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number listed below.

The Office is hereby authorized to charge any fees, or credit any overpayments, to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: June 8, 2005

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